Figure 1. Physical photo of TEC5V6A-NT

FEATURES

- High Efficiency: ≥90%
- Maximum Output Current: 6A
- Maximum Output Voltage: $\pm V_{VPS}$
- Actual Object Temperature Monitoring
- High Stability: 0.01°C
- High Reliability
- Zero EMI
- Compact Size
- 100 % lead (Pb)-free and RoHS compliant

DESCRIPTION

The TEC5V6A-NT is an electronic module designed for driving TECs (Thermo-Electric Coolers) with high stability in regulating the object temperature, high energy efficiency, zero EMI, and small package. It can be used in a vacuum environment. Figure 1 is the photo of the actual TEC5V6A-NT.

This module provides interface ports for users to set the desired object temperature, i.e. set-point temperature; the maximum output voltage across TEC; and the compensation network. The compensation network compensates the high order thermal load and thus stabilizes the temperature control loop.

It provides these functions: thermistor T-R curve linearization, temperature measurement and monitoring, temperature control loop status indication, TEC voltage monitoring, power up delay, and shut down.

The TEC5V6A-NT comes with a high stability low noise 3.0V voltage reference which can be used for setting the desired object temperature by using a POT (Potentiometer) or a DAC (Digital to Analog Converter). When using this reference for setting the set-point temperature, the set-point temperature error is independent of this reference voltage. This is because the internal temperature measurement network also uses this voltage as the reference, the errors in setting the temperature and measuring the temperature cancel with each other, setting the object temperature with higher stability. This reference can also be utilized by an ADC (Analog to Digital Converter), for the same reason, the measurement error will also be independent of the reference voltage, resulting in a more accurate measurement.

Figure 2 is the real size top view of the controller showing the pin names and locations with the actual size. TEC5V6A-NT pin functions are shown in Table 1.

Warning: This controller module can only be soldered manually on the board by a solder iron of < 310°C (590°F), it cannot go through a reflow oven process.

The TEC5V6A-NT is packaged in a 6 sided metal enclosure, which blocks EMIs (Electro-Magnetic Interferences) to prevent the controller and other electronics from interfering with each other.

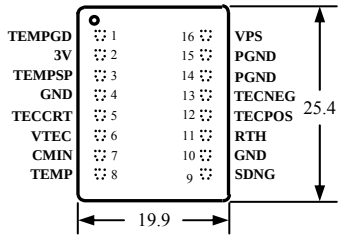

Figure 2. Pin names and locations

SPECIFICATIONS

Table 1 Pin Function Descriptions

Pin #	Pin Name	Type	Description
1	**TEMPGD**	Digital output	Temperature good indication. It is pulled high when the set-point temperature and the actual desired object temperature are <0.1°C in temperature difference when the set-point temperature range is 20°C; or <3mV in voltage difference between the voltages of TEMP and TEMPSP nodes. On this pin, there is an internal pull up resistor of 10k tied to the VPS rail. When going low, this pin is pulled down by an open drain FET with a resistance of 250Ω @ V_{VPS} = 5V. ***A 100nF capacitor to GND** needs to be added to this TEC controller manufactured before March 27th, 2012. Otherwise, there will be an interference of Vp-p=200mV, f=500kHz.
2	**3VR**	Analog output	Reference voltage output, 3V. It can be used by a POT or DAC for setting the set-point temperature voltage on the TEMPSP pin and/or a DAC for measuring the temperature through the TEMP pin. The maximum sourcing current capability is 1.5mA and the maximum sinking is 4mA with a stability of <50ppm/°C max.
3	**TEMPSP**	Analog input	Object set-point temperature input port. It is internally tied by a 10MΩ resistor to the half value of the reference voltage, 1.5V. It is highly recommended to set this pin's voltage by using the controller's voltage reference. The lower limit of the setting voltage for this pin is 0.1V. Setting this pin to a <0.1V voltage may cause the controller over cooling the object. This pin can also be set to a voltage that is about 0.2V away from the VPS rail. This pin can be set by using a POT or DAC.
4	**GND**	Ground	Signal ground for the POT, ADC, DAC and the thermistor, see Figure 4.
5	**TECCRT**	Both analog input and output	TEC control voltage. It can be left unconnected or used to control the TEC voltage directly. Set TECCRT between 0V to VPS, the voltage across TEC will be: TEC voltage = $V_{VPS} - 2\times V_{TECCRT}$. It can also be used to configure the maximum voltage cross the TEC: Max. TEC voltage = $V_{VPS}\times Rm/(Rm+10k)$, where Rm is the resistance of the two resistors one between TECCRT to GND and the other between TECCRT to VPS, see Figure 4.
6	**VTEC**	Analog output	TEC voltage indication. TEC voltage = [max. TEC voltage]×[$V_{VPS} - 2\times V_{VTEC}$]/$V_{VPS}$. When TECCRT is used to control the TEC voltage directly, measure TECCRT to derive the TEC voltage instead, and use this formula: TEC voltage = $V_{VPS} - 2\times V_{TECCRT}$. The maximum driving current of pin **VTEC** is 30mA and the output voltage swing is 0V to V_{VPS}.
7	**CMIN**	Analog input	Compensation input pin for the thermal control loop. Leave it open in production. When prototyping, use this pin with a tuner on the evaluation board, TECEV104 (produced by ATI) to tune the compensation network to match the characteristics of the thermal load.
8	**TEMP**	Analog output	Actual object temperature. It swings from 0V to V_{VPS}, corresponds to 15°C to 50°C when V_{VPS} equals to 5V. See the curve below.
9	**SDNG**	Digital input	Shut down control. When pulled low, it shuts down the controller. Leave it open or pull it high to activate the controller. The threshold voltage is 1.4V. This pin is internally pulled up by a resistor of 100k to VPS.
10	**GND**	ground	Signal ground, internally connected to Pin 4 GND. Can be used for connecting the thermistor
11	**RTH**	Analog input	Inverting input to error amplifier.
12	**TECPOS**	Analog power output	Connects to TEC positive terminal

13	**TECNEG**	Analog power output	Connects to TEC negative terminal
14	**PGND**	Power ground	Power ground for connecting to the power supply
15	**PGND**	Power ground	Power ground for connecting to the power supply, internally connected with pin 14
16	**VPS**	Power input	Positive power supply rail. The value is 5V.

Table 2. Characteristics ($T_{ambient}$=25°C)

Parameter	Test Conditions	Value	Unit/Note
Object* temp. stability vs. ambient temp	V_{VPS}=5V, R_{LOAD}=0.8Ω	0.0002	°C/°C
Object temp. vs. set-point offset	$T_{AMBIENT}$ is 0 ~ 50°C, set-point temp. is 15°C ~35°C	±0.1°C or ±15mV	
Object temp. response time	≤0.1 to the set-point temperature at a 1°C step	<5	s
Efficiency	V_{VPS}=5V, R_{LOAD}=0.8Ω	≥90%	-
Max. output current	V_{VPS}=5V, R_{LOAD}=0.8Ω	6	A
Max. output voltage	V_{VPS}=5V, R_{LOAD}=0.8Ω	0 ~ V_{VPS}-0.3	V
PWM frequency		500	kHz
Power supply voltage	—	4.5 ~ 5.5 (specify 5V)	V
Set-point temp.** control voltage	V_{IN}=5V, R_{LOAD}=0.8Ω	0.1 ~ V_{VPS}	V
Default set-point temp. range***	V_{VPS}=3V	15 ~ 35	°C
Operating temp. range	V_{IN}=5V, R_{LOAD}=0.8Ω	−40 ~ 85	°C
Storage temp. range		−55 ~ 125	°C

* Object temperature refers to the actual cold side temperature of the TEC, on where the object is mounted.

** Set-point temperature is the temperature desired to have on the object.

*** Can be customized to any range according to requirement.

**** This TEC controller can only drive the TECs having > 1Ω impedance, which equals V_{MAX}/I_{MAX}.

***** After many experiment, according to the parameter and the figuring method of R_{load}, we advise customers to use R_{LOAD} of 0.8Ω. We advise customers to use voltage of 6V as the power supply.

BLOCK DIAGRAM

The block diagram of the controller is shown in Figure 3.

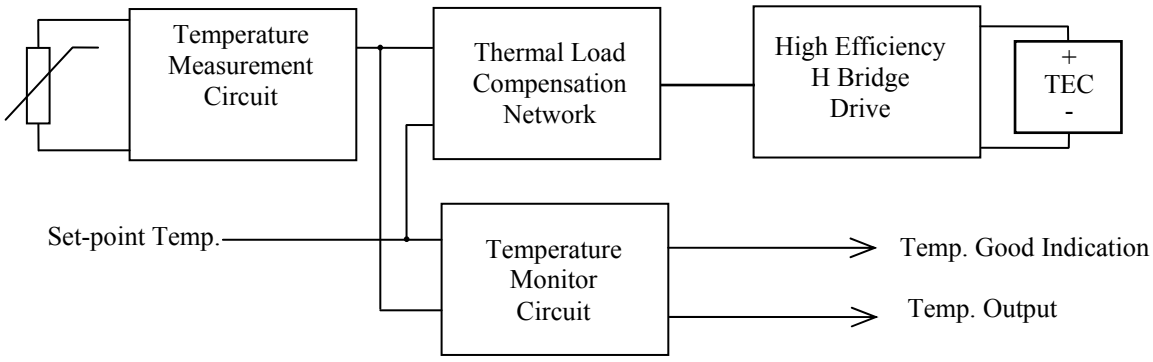

Figure 3. TEC Controller Block Diagram

APPLICATIONS

TEC controller connections are shown in Figure 4.

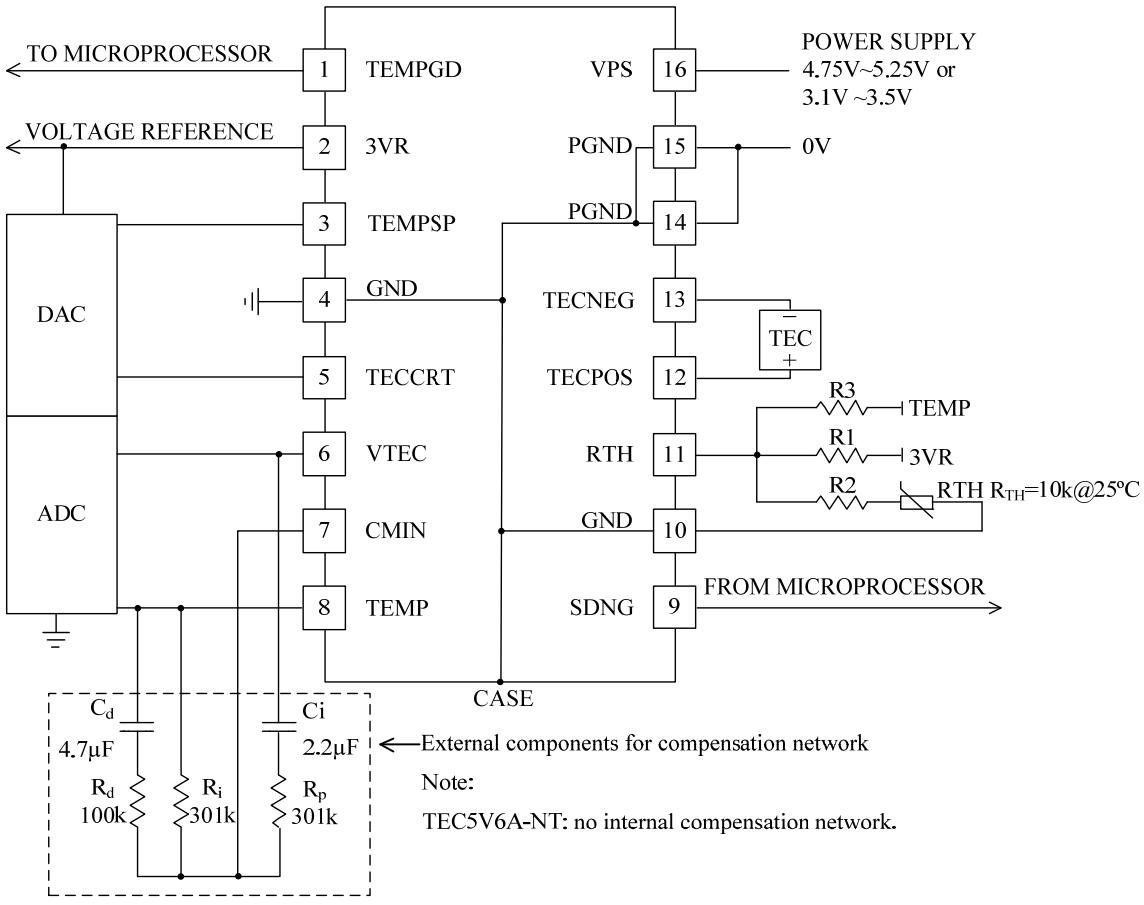

Figure 4. TEC Controller Connections

If you want to use this TEC controller for other applications not discussed here, such as use it with wave locker controllers, please consult us. The same as to other customizations, such as setting the TEMPSP by using a voltage source swings above 3V and/or V_{VPS}.

The TEC controller doesn't come with a default temperature setting network, which allows you to specify the temperature range by using the external resistors, R1, R2 and R3.

Note: This TEC controller doesn't come with an internal compensation network and we don't recommend using internal compensation network either. Implementing the network externally is highly recommended since it can be modified for driving different thermal load and/or the thermal load characteristics is not certain or fixed at the early design stage.

Using TEC Controllers for Driving A Heater

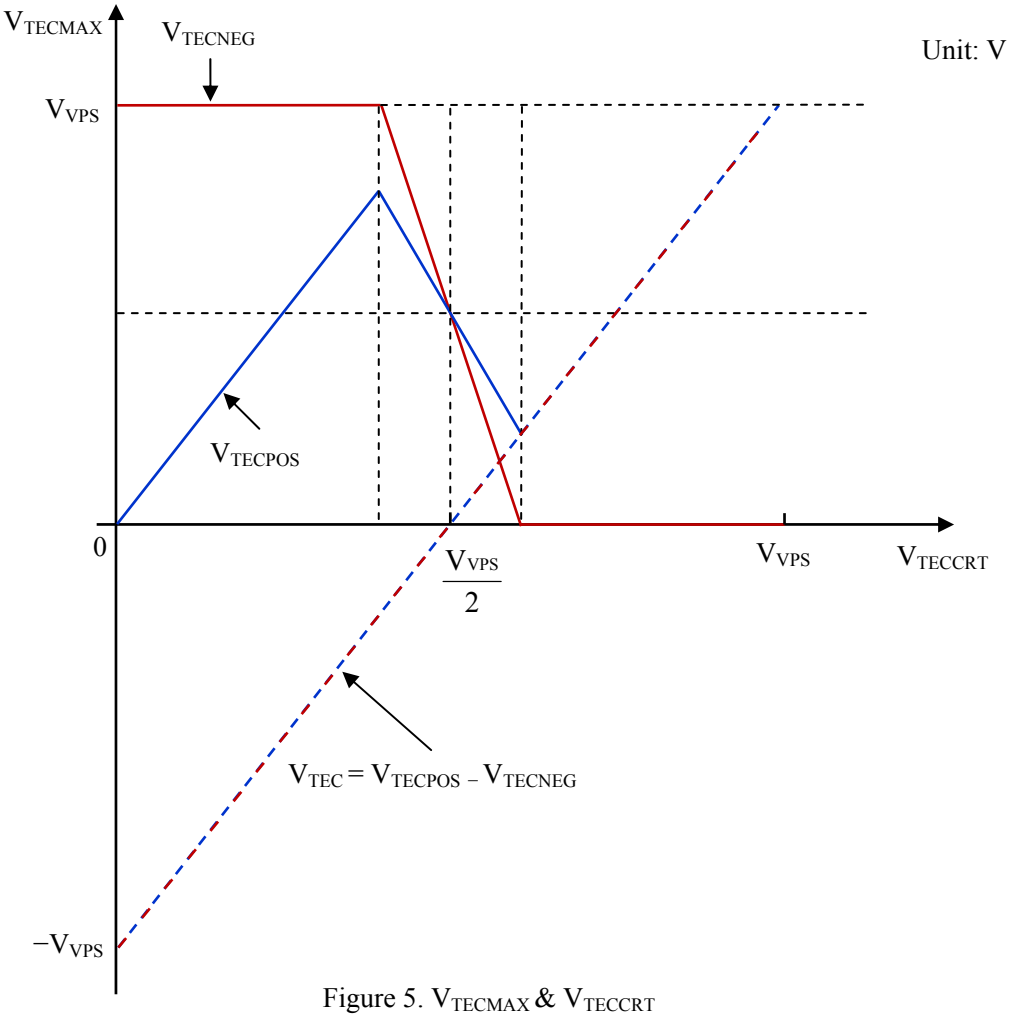

Figure 5. V_{TECMAX} & V_{TECCRT}

V_{TEC} & V_{TMO} WAVEFORMS

The V_{TEC} and V_{TMO} waveforms are shown in Figure 6, which change with V_{RTH}. We can see that there is no overshoot in the waveforms. V_{RTH} changes little, so there's no waveform shown. Figure 7 shows the connection method.

Compensation network: C_d=16.9uF, R_d=12.4k, R_i=1.872M, R_p=1.373M, C_i=1.69uF.

Note: Ch1: V_{TMO}; Ch2: V_{VTEC}

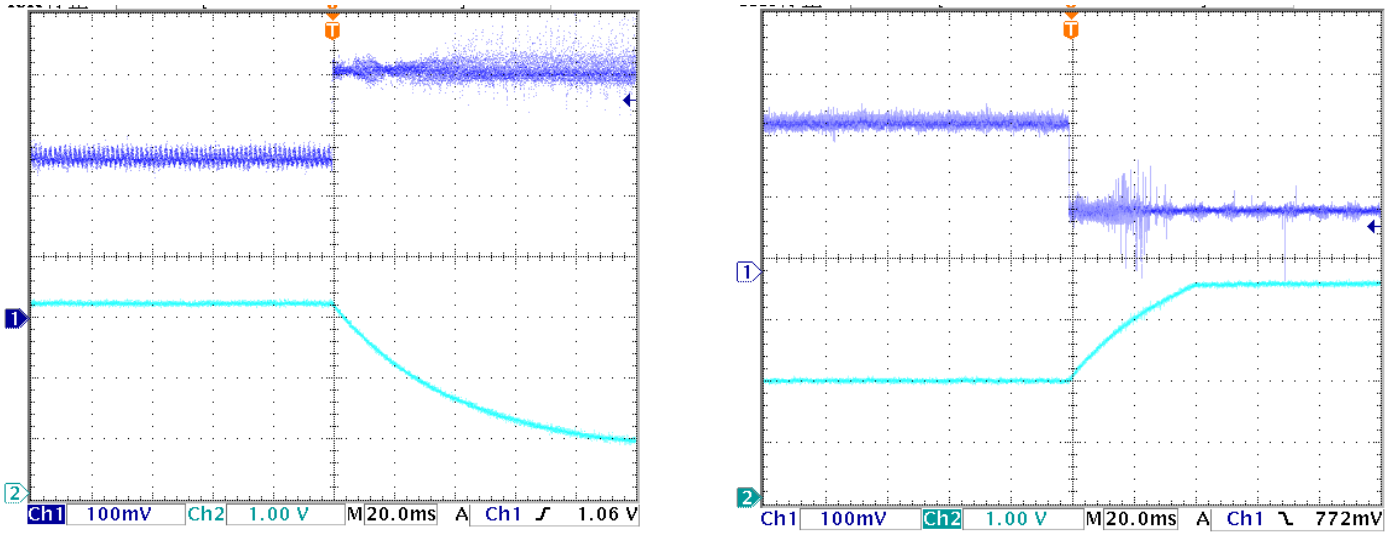

Figure 6. V_{TEC} & V_{TMO} Waveforms

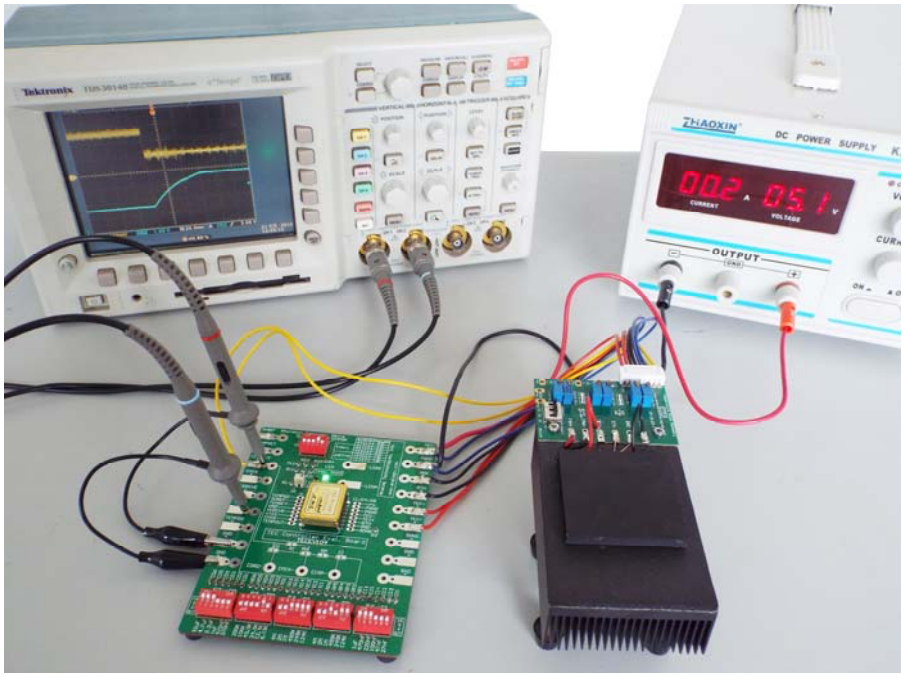

Figure 7. Connection Method

TEMPGD INTERNAL CIRCUIT

When temperature difference between the actual temperature and the set-point temperature < 0.1°C, the pull-up resistor R1 of TEMPGD is 130Ω; When temperature difference between the actual temperature and the set-point temperature > 0.1°C, the pull-down resistor R2 of TEMPGD is 12.7Ω. See Figure 8.

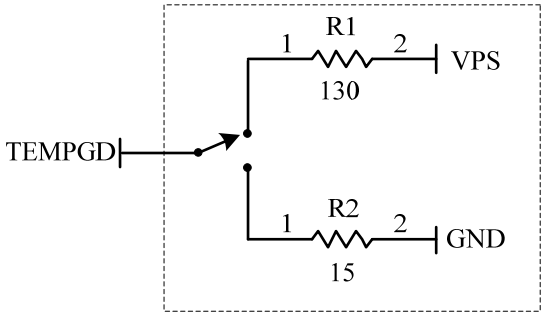

Figure 8. Internal Equivalent Circuit on TEMPGD Pin

NOTE: The power supply may have overshoot, when happens, it may exceed the maximum allowed input voltage, 6V, of the controller and damage the controller permanently. To avoid this from happening, do the following:

1. **Connect the controller solid well with the power supply before turning on the power.**
2. **Make sure that the power supply has sufficient output current. It is suggested that the power supply can supply 1.2 to 1.5 times the maximum current the controller requires.**
3. **When using a bench top power supply, set the current limit to >1.5 times higher than the maximum current the controller requires.**

SPECIAL NOTE

If you experience a high current spike when you change TEMPSP voltage quickly by a large amount, such as > 0.1V, a capacitor of 1uF can be added between TECCRT and GND. For TEC controllers manufactured after Nov. 10, 2015, there is no such a problem.

MECHANICAL DIMENSIONS

Dimensions of the DIP package controller is shown in Figure 9.

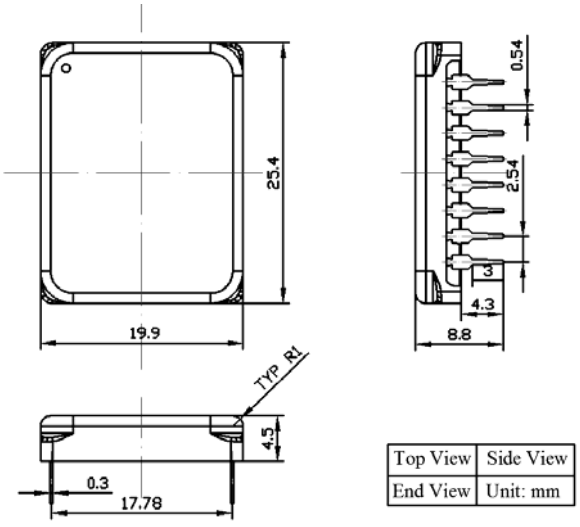

Figure 9. Dimensions of the DIP package controller of TEC5V6A-NT

WARNING: Both the surface mount and the through hole types of modules can only be soldered manually on the board by a solder iron of < 310°C (590°F), they cannot go through a reflow oven process.

ORDERING INFO

Table 3.

Part #	Description
TEC5V6A-NT	TEMP =On @SDNG = 0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network

SELECTION GUIDE

Part #	V_{IN}	V_{OUT}	Dimensions (mm)	Difference
TEC14M5V3R5AS	2.7V ~ 5.5V	$\pm V_{VPS}$	14.0×14.0×2.2	Micro TEC controller
TEC18V15A	6.0V~18V	±15V	35.7×35.7×7.2	High voltage high current with embedded firmware inside
TEC50V20ACH Under Development	12V ~ 50V	±40V	63.0×61.0×16.7	High voltage high current
TEC5V6A-D	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = On @SDNG= 0 TECNEG: Linear; TECPOS: Filtered PWM; Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 5mV$
TEC5V6A-DA	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = On @SDNG = 0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 2mV$
TEC5V6A-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = On @ SDNG= 0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 0.5mV$
TEC5V6A-NT	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP =On @SDNG = 0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network
TEC5V4A-D	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = On @SDNG = 0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 5mV$
TEC5V4A-DA	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = On @SDNG = 0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 2mV$
TEC5V4A-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = On @SDNG = 0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$
TEC5V4A-NT	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = On @SDNG = 0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network

TECA1-xV-xV-DAH	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = Off @SDNG = 0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \le 0.5mV$
TECA1-xV-xV-DAH-OP	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = Off @SDNG = 0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: removed
TECA1LD-xV-xV-DAH	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = Off @SDNG = 0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed With internal compensation network
TECA1-xV-xV-D	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = Off @SDNG = 0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP - VTEMPSP}\rvert \le 5mV$
TECA1-xV-xV-D-OP	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = Off @SDNG = 0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: removed
TECA1LD-xV-xV-D	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = Off @SDNG= 0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed With internal compensation network
TECA1-5V5V-NT	5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP = Off @SDNG = 0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network
TECA2-xV-xV-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	20.14×14.6×8.0	TEMP = Off @SDNG = 0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed Smaller size

NOTICE

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