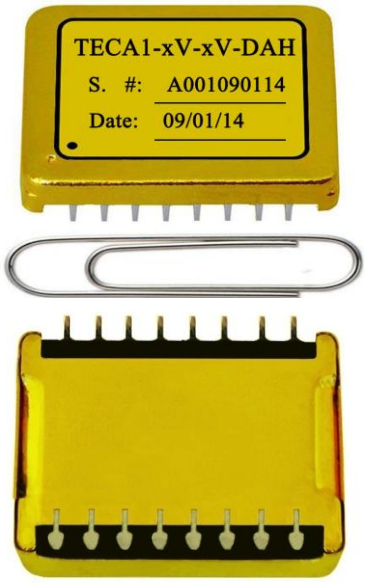


Figure 1. The Photos of Actual TECA1-xV-xV-DAH

## FEATURES

- High Efficiency: ≥90%
- Maximum Output Current: 2.5A
- Actual Object Temperature Monitoring
- High Stability: 0.004°C
- High Reliability and Zero EMI
- Compact Size
- 100 % lead (Pb)-free and RoHS compliant

## DESCRIPTION

The TECA1-xV-xV-DAH is an electronic module designed for driving TECs (Thermo-Electric Coolers) with high stability in regulating the object temperature, high energy efficiency, zero EMI, and small package. It can be used in a vacuum environment. Figure 1 is the photo of an actual TECA1-xV-xV-DAH TEC controller.

This module provides interface ports for users to set the desired object temperature, i.e. set-point temperature; the maximum output voltage across TEC; and the compensation network. The compensation network compensates the high order thermal load and thus stabilizes the temperature control loop.

It provides these functions: thermistor T-R curve linearization, temperature measurement and monitoring, temperature control loop status indication, TEC voltage monitoring, power up delay, and shut down.

The TECA1-xV-xV-DAH comes with a high stability low noise 3.0V voltage reference which can be used for setting the desired object temperature by using a POT (Potentiometer) or a DAC (Digital to Analog Converter). When using this reference for setting the set-point temperature, the set-point temperature error is independent of this reference voltage. This is because the internal temperature measurement network also uses this voltage as the reference, the errors in setting the temperature and measuring the temperature cancel with each other, setting the object temperature with higher stability. This reference can also be utilized by an ADC (Analog to Digital Converter), for the same reason, the measurement error will also be independent of the reference voltage, resulting in a more accurate measurement.

Table 1 shows the difference between TECA1-xV-xV-D and TECA1-xV-xV-DAH.

Table 1.

| Part # | Maximum $\lvert V_{TEMP} - V_{TEMPSP} \rvert$ (mV) |
|---|---|
| TECA1-xV-xV-DAH | ≤0.5 |
| TECA1-xV-xV-D | ≤5 |

Figure 2 is the real size top view of the controller showing the pin names and locations. The functions of all the pins are shown in Table 2.

**Warning: This controller module can only be soldered manually on the board by a solder iron at < 310°C (590°F), it cannot go through a reflow oven process.**

The TECA1-xV-xV-DAH is packaged in a 6 sided metal enclosure, which blocks EMIs (Electro-Magnetic Interferences) to prevent the controller and other electronics from interfering with each other.

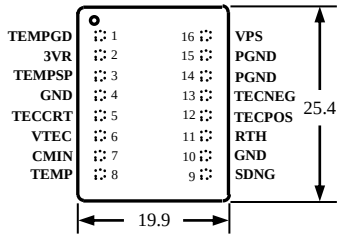


Figure 2. Pin names and Locations

The TECA1-xV-xV-DAH TEC controller can come with an internal compensation network for stabilizing the temperature control loop. The compensation network with the default values shown in Figure 4 matches most of the commonly used butter-fly packaged TEC thermal loads. The part number TECA1LD-xV-xV-DAH, with the "LD" suffix, stands for the controller with an internal compensation network; while the part number TECA1-xV-xV-DAH, without the "LD" suffix, stands for the controller without the internal compensation network and external compensation network will be required for the controller to operate. The compensation network is made of 5 components: 3 resistors and 2 capacitors. This network can be implemented either internally by embedding them into the controller circuitries inside the controller enclosure or externally by soldering the 5 components on the PCB (Printed Circuit Board) on which the TEC controller is mounted. Implementing the network externally is highly recommended since it can be modified for driving different thermal load and/or the thermal load

characteristics is not certain or fixed at the early design stage. The part number TECA1LD-xV-xV-DAH denotes the controller with an internal compensation network, the values of the components in the network are either the default values shown in Figure 4 or the values specified in the part number, the naming rules are shown in Table 4.

## SPECIFICATIONS

Table 2. Pin Function Descriptions

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1 | **TEMPGD** | Digital output | Temperature good indication. It is pulled high when the set-point temperature and the actual desired object temperature are <0.1°C in temperature difference when the set-point temperature range is 20°C; or <0.5mV in voltage difference between the voltages of TEMP and TEMPSP nodes. It is internally pulled up or down a 130Ω and a 90Ω resistor respectively when goes up and down. It can be used to drive LEDS as indications. |
| 2 | **3VR** | Analog output | Reference voltage output, 3V. It can be used by a POT or DAC for setting the set-point temperature voltage on the TEMPSP pin and/or a DAC for measuring the temperature through the TEMP pin. The maximum sourcing current capability is 1.5mA and the maximum sinking is 4mA with a stability of <50ppm/°C max. |
| 3 | **TEMPSP** | Analog input | Object set-point temperature input port. It is internally tied to a voltage divider formed by two 100kΩ resistors to reduce the reference by half, equals to 1.5V. The open circuit voltage of this pin is thus 1.5V, corresponding to a set-point temperature of 25°C by using the default temperature network (with the set-point temperature range being from 15°C to 35°C. It is highly recommended to set this pin's voltage by using the controller's voltage reference. The lower limit of the setting voltage for this pin is 0.1V. Setting this pin to a <0.1V voltage may cause the controller over cooling the object. This pin can also be set to a voltage that is about 0.2V away from the VPS rail. For example, when $V_{VPS}$ = 5V, this pin can be set up to $V_{VPS}$ – 0.1V, corresponding to approximately 50°C in temperature when the default temperature network is in place, see the curve shown in Figure 13. This pin can be set by using a POT or DAC. When the set-point temperature needs to be at 25°C, leave this pin unconnected. |
| 4 | **GND** | Ground | Signal ground for the POT, ADC, DAC and the thermistor, see Figure 4. |
| 5 | **TECCRT** | Both analog input and output | TEC control voltage. It can be left unconnected or used to control the TEC voltage directly. Set TECCRT between 0V to $V_{VPS}$, the voltage across TEC will be:<br>TEC voltage = $V_{VPS} - 2 \times V_{TECCRT}$.<br>It can also be used to configure the maximum voltage cross the TEC:<br>Max. TEC voltage = $V_{TEC\_Max} \times Rm / (Rm+10k)$,<br>where $V_{TEC\_Max}$ is the maximum output voltage of the TEC controller configured by the internal limiting circuit when the controller is released by the factory, it is marked on the TEC controller label;<br>Rm is the resistance of the two resistors one between TECCRT to GND and the other between TECCRT to $V_{VPS}$, as shown in Figure 4.<br>When the resistors Rm are in place, the TECCRT pin is used for controlling the TEC voltage directly. This pin can be utilized for monitoring the voltage across the TEC:<br>TEC voltage = (Max. TEC voltage) $\times (1 - 2 \times TECCRT/V_{VPS})$.<br>The output impedance of this pin is 5k. |
| 6 | **VTEC** | Analog output | TEC voltage indication. When the Rm's mentioned above or the TECCRT is not used for controlling the output TEC voltage directly, this pin can be utilized for monitoring the output voltage across the TEC: TEC voltage = (Max. TEC voltage) $\times (1 - 2 \times V_{TEC}/V_{VPS})$. The maximum driving current of this pin is 30mA and the output voltage swing is 0V to $V_{VPS}$. |

| | | | |
|---|---|---|---|
| 7 | **CMIN** | Analog input | Compensation input pin for the thermal control loop. Connect the compensation network to this pin as shown in Figure 4 or leave it unconnected if the TEC controller has an internal compensation network already.<br>This pin is noise sensitive. Do not connect this pin with a long wire in the air or long trace on the PCB when layout the board for the TEC controller. |
| 8 | **TEMP** | Analog output | Actual object temperature indication. It swings from 0V to $V_{VPS}$. By a default internal temperature network, it represents 15°C to 35°C when this pin's voltage swings 0V to 3V linearly; when changing from 0V to 5V, it represents 15°C to 50°C in temperature, see Figure 13. |
| 9 | **SDNG** | Digital input | Shut down control. When pulled low, it shuts down the controller. Leave it open or pull it high to activate the controller. The threshold voltage is 1.4V. This pin is internal pull up by a resister of 100k to $V_{VPS}$. The threshold voltages of this pin are:<br>before shuts down, the quiescent current is about 45mA; when going down, SDNG = 1.36V shuts down the TECNEG output stage and the quiescent current becomes 26mA; SDNG = 0.8V shuts down TECPOS output stage and the quiescent current becomes 6mA; when going up, SDNG = 1.0V activate the TECPOS output stage and the quiescent current goes back to 26mA; SDNG = 1.37V activates the TECNEG output stage and the quiescent current goes back to the full normal value of 45mA. The maximum input voltage range allowed on this pin is from 0V to 6V.<br>**Please note** that for all the controllers manufactured **before** Dec. 2010, when $V_{SDNG}$=0, only TEMP works. And for the controllers manufactured **after** Dec. 2010, when $V_{SDNG}$=0, all the pins including TEMP will not work. |
| 10 | **GND** | ground | Signal ground, internally connected to Pin 4 GND. It can be used for connecting the return pass of the thermistor. |
| 11 | **RTH** | Analog input | Connect to the thermistor for sensing the object temperature. By using the default temperature network that comes with the standard TEC controller, the thermistor is expected to have a 10kΩ @ 25°C and the R-T curve data are given in Figure 9. It's recommended to use our ntc thermistor, ATH10K1R25. |
| 12 | **TECPOS** | Analog power output | Connects to TEC positive terminal |
| 13 | **TECNEG** | Analog power output | Connects to TEC negative terminal |
| 14 | **PGND** | Power ground | Power ground for connecting to the power supply |
| 15 | **PGND** | Power ground | Power ground for connecting to the power supply, internally connected with pin 14 |
| 16 | **VPS** | Power input | Positive power supply rail. Two possible values: 3.3V and 5V, depending on the module. |

Table 3. Characteristic ($T_{Ambient}$=25°C)

| Parameter | Test Condition | Value | Unit/Note |
|---|---|---|---|
| Object* temp. stability vs. ambient temp. | $V_{VPS}$ = 5V, $R_{LOAD}$ = 2Ω | 0.0002 | °C/°C |
| Offset Object temp. vs. set-point temp. | $T_{Ambient}$ is 0~50°C Set-point temp. is 15°C ~35°C | ±0.004°C or ±0.5mV | TECA1-xV-xV-DAH |
| | | ±0.1°C or ±5mV | TECA1-xV-xV-D |
| Maximum $\lvert V_{TEMP} - V_{TEMPSP} \rvert$ | $V_{VPS}$ = 5V, $V_{VTEC}$= 4V, $R_{LOAD}$ = 2Ω | ≤0.5mV | TECA1-xV-xV-DAH |
| | | ≤5mV | TECA1-xV-xV-D |
| Object temp. response time | ≤0.1 to the set-point temp. at a 1°C step | <5 | s |
| Efficiency | $V_{VPS}$ = 5V, $R_{LOAD}$ = 2Ω | ≥90% | — |
| Max. output current | $V_{VPS}$ = 5V, $R_{LOAD}$ = 2Ω | 2.5 | A |
| Max. output voltage | $V_{VPS}$ = 5V, $R_{LOAD}$ = 2Ω | 0 ~ $V_{VPS}$ | V |
| Shutdown current | $V_{VPS}$ = 5V, $V_{SDNG}$ = 0V | 6.8 | mA |
| PWM frequency | | 500 | kHz |
| Power supply voltage | — | 3.2 ~ 3.5 or 4.5 ~ 5.5 (Typically 3.3 or 5 ) | V |
| Set-point temp.** control voltage | $V_{VPS}$ = 5V, $R_{LOAD}$ = 2Ω | 0.1 ~ $V_{VPS}$ | V |
| Default set-point temp. range*** | $V_{VPS}$ =3V | 15 ~ 35 | °C |
| Operating temp. range | $V_{VPS}$ = 5V, $R_{LOAD}$ = 2Ω | −40 ~ 85 | °C |

* Object temperature refers to the actual temperature of the object which is mounted on the cold side the TEC and its temperature needs to be regulated by the TEC. This object is often a metal block on which a laser diode or an optical crystal is mounted.

** Set-point temperature is the temperature of the object desired to achieve.

*** Can be customized to any range according to requirement.

**** This TEC controller can only drive the TECs having > 1Ω impedance, which equals $V_{MAX}/I_{MAX}$.

***** After many experiments, according to the parameter and the figuring method of $R_{LOAD}$, we advise customers to use $R_{LOAD}$ of 2Ω to get the ideal character. We can also make the Maximum Output Voltage reach any value of ($V_{VPS}$ – 0.1×$I_{OUT}$) if you need.

## BLOCK DIAGRAM

The block diagram of the controller is shown in Figure 3.

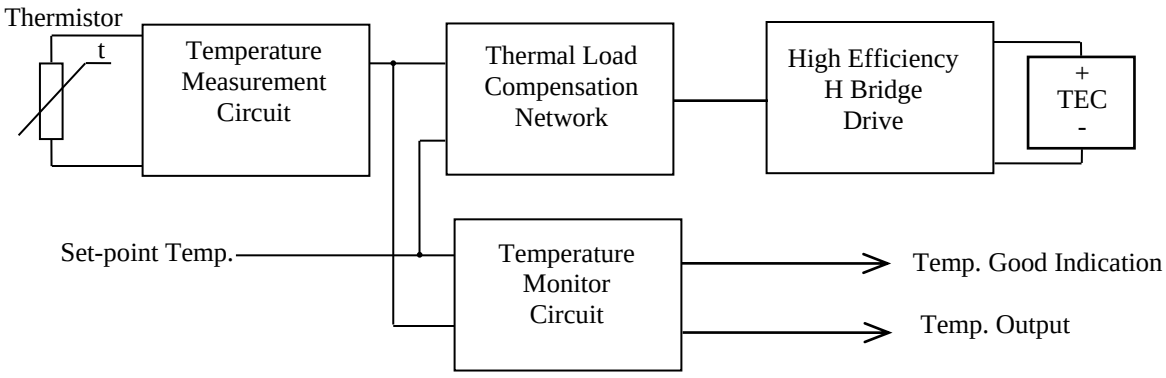


Figure 3. TEC controller block diagram

## APPLICATIONS

TEC controller connections are shown in Figure 4.

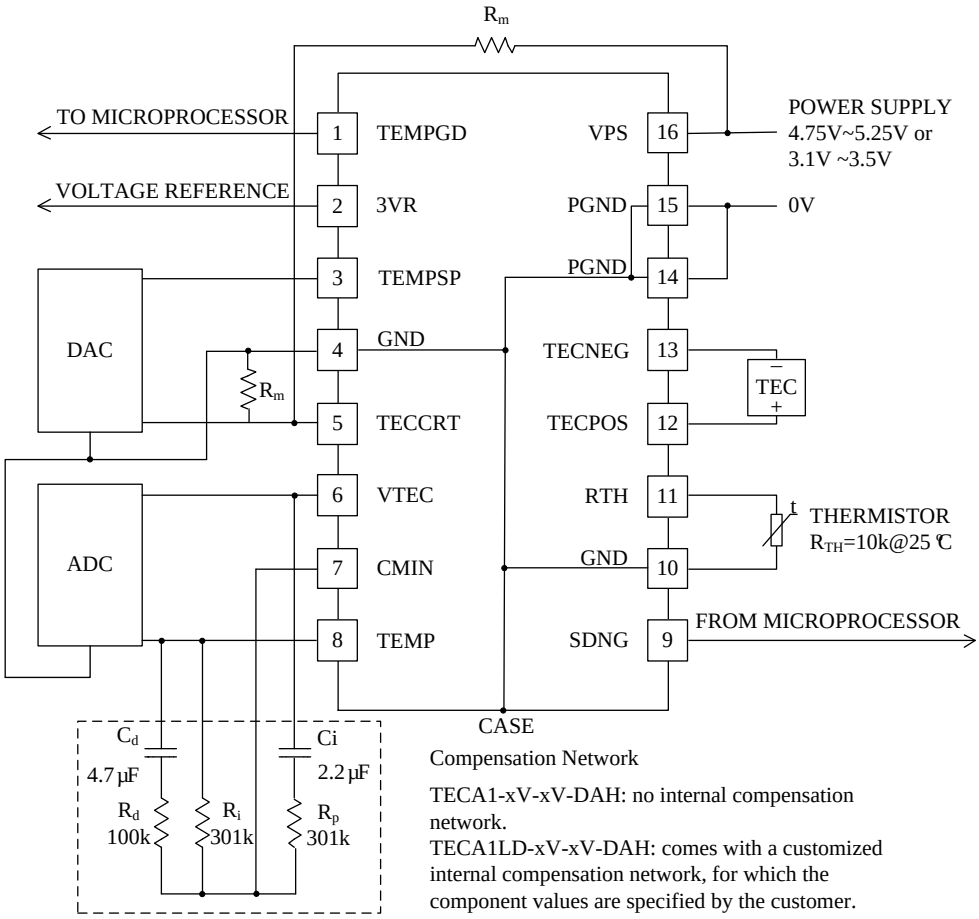


Figure 4. Microprocessor Based Application Circuit

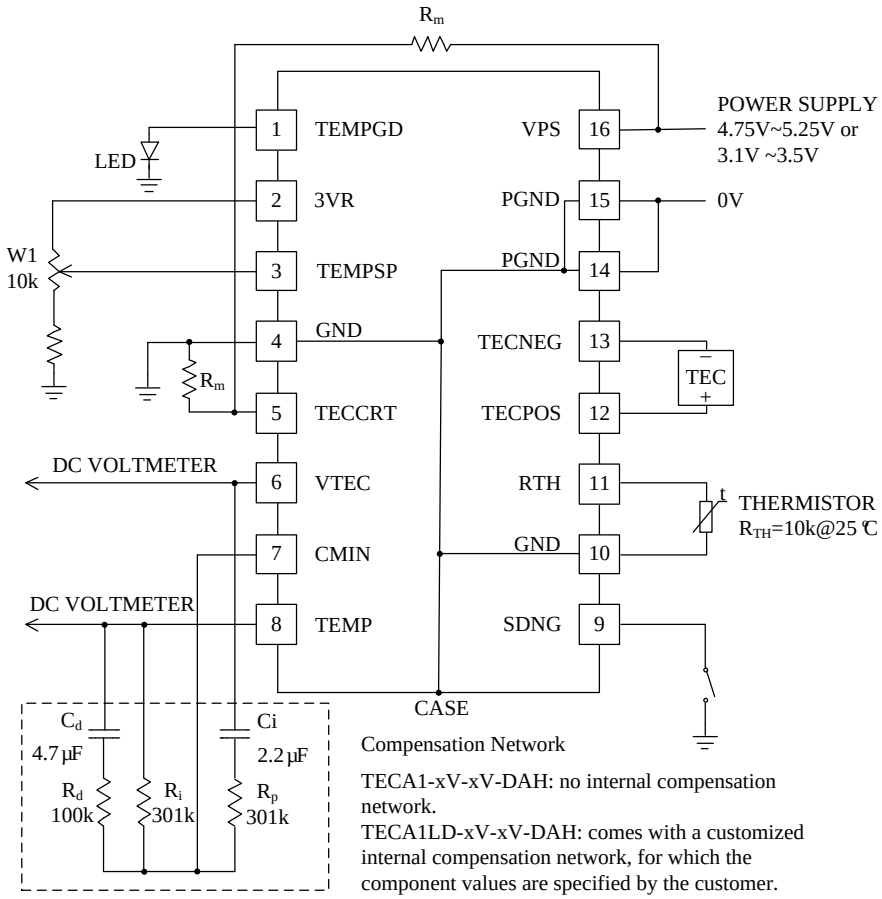


Figure 5. Stand-Alone Application Circuit

When the TEC controller is used stand-alone, using a POT or a pair of resistors to replace the POT to set the voltage for the set-point temperature pin TEMPSP as shown in Figure 5. The input voltage range on the TEMPSP pin must be >0.1V and the maximum voltage on this pin is $V_{VPS}$ – 0.1V. The VTEC can be utilized for measuring the voltage across the TEC as described in Table 3. The actual object temperature can be monitored by measuring the voltage on the TEMP pin. The relationship between the actual temperature and the TEMP voltage is determined by the internal temperature network. When using the default temperature network, the relationship is shown in Figure 5, the approximate formula is:

$$ß = \log_{10}(R_oT_1/R_oT_2) / [(1/T_1 - 1/T_2) \times \log_{10}e]$$

$R_oT_1$ stands for the zero power resistance at absolute temperature $T_1$

$R_oT_2$ stands for the zero power resistance at absolute temperature $T_2$

$T_1$ is the temperature 1, expressed in degree Kelvin.

$T_2$ is the temperature 2, expressed in degree Kelvin.

The maximum error between the actual output voltage and approximated voltage is 0.013V, equivalent to 1.3% error.

If this TEC controller is to be used for other applications not discussed here, such as use it with wave locker controllers, please consult with us and we can help. The same as to other customizations, such as setting the **TEMPSP** by using a voltage source swinging above 3V and/or $V_{VPS}$. This TEC controller comes with a default temperature setting network, it sets the set-point temperature to be between 15°C to 35°C when setting the TEMPSP pin voltage to be between 0V to 3V linearly and using a specific de-facto "standard" 10k @ 25°C thermistor, with its R-T value data listed in Figure 10 and Table 4. When using different thermistors and/or needing different set-point temperature ranges, please contact us, we will configure the internal temperature network for you.

In order to change the set-point temperature, an external resistor can be used to combine with your thermistor to make it equal to 10kΩ. For example, at 4°C, the thermistor is about 25kΩ, add another resistor in parallel, therefore, the total resistance is 10kΩ. After this, set the set-point temperature pin, TEMPSP, to 1.5V, the actual set-point temperature will be about 4°C. At 37°C, the thermistor is about 5kΩ, put an external resistor 5kΩ in series with this thermistor, therefore, the total resistance will be about

10kΩ at 37°C. Now, set TEMPSP pin to 1.5V, the actual set-point temperature will be about 37°C.

When using, users need to connect the pins of VTEC and CMIN together. Connect the TEMPSP pin to DAC. About ADC, users can figure it yourself.

**Note**: A socket strip can be used for mounting this TEC controller. More detail technical data about this socket can be found here: http://www.digikey.com/product-detail/en/SS-132-G-2/SAM1115-32-ND/1105559

**Using TEC Controllers for Driving A Heater**

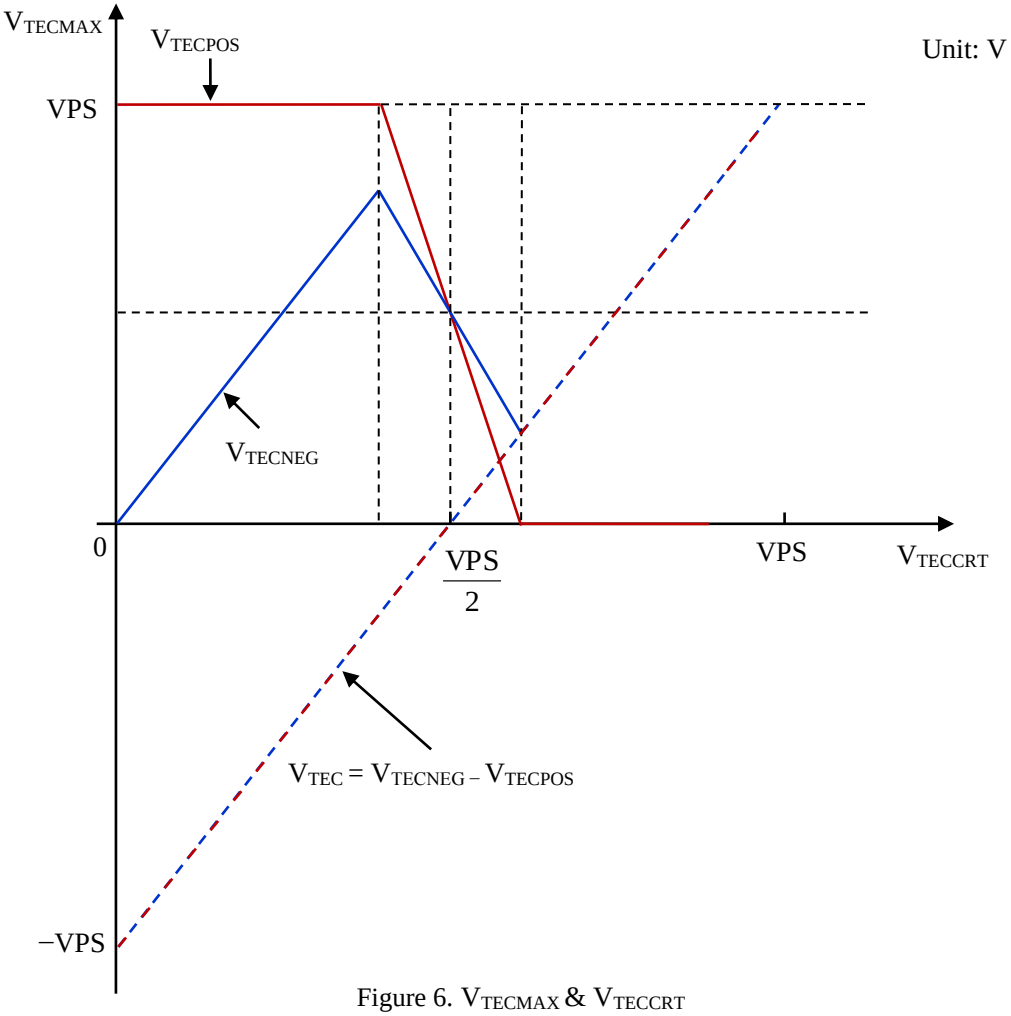


Figure 6. $V_{TECMAX}$ & $V_{TECCRT}$

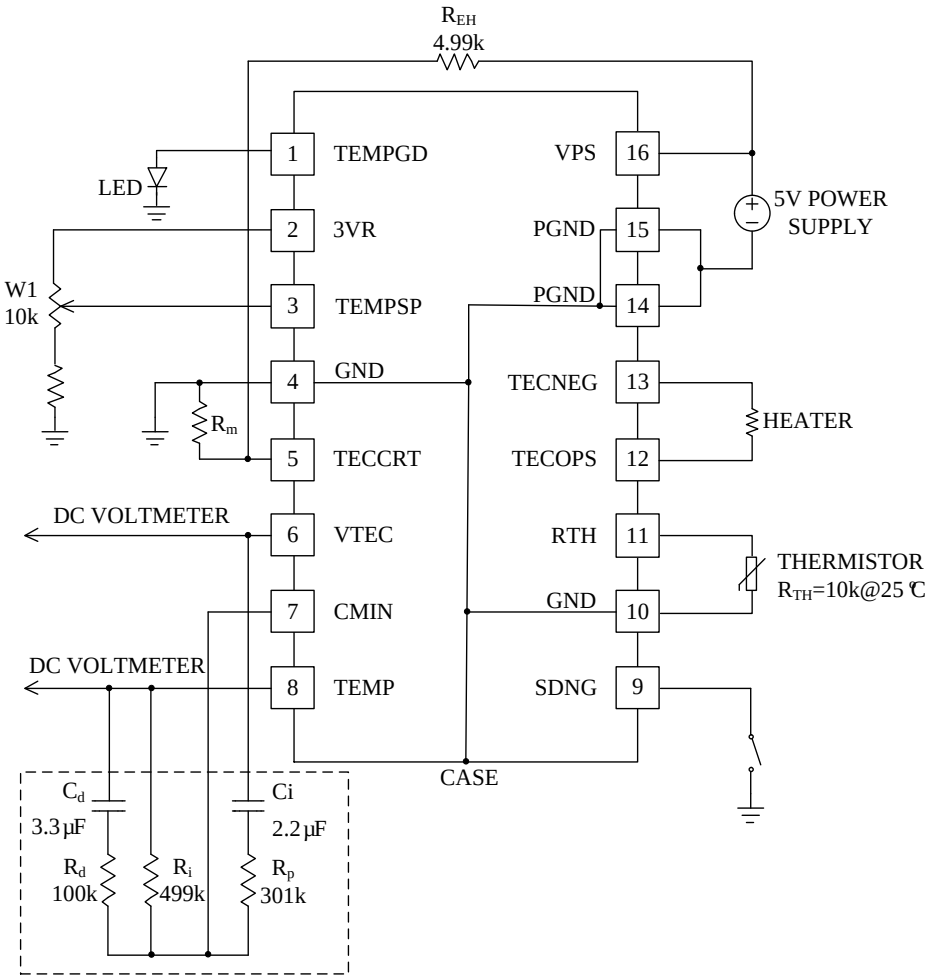


Figure 7. Driving a Heater for <3.3V @ ≤3A

If $V_{HTMAX}$<3.3V, the part # is TECA1-5V-[$V_{HTMAX}$]V-D. For example, $V_{HTMAX}$=2.5V, the part number will become: TECA1-5V-2.5V-D, when using a 5V power supply. If powered by a 3.3V power supply, the part number will be: TECA1-3V-2.5V-D.

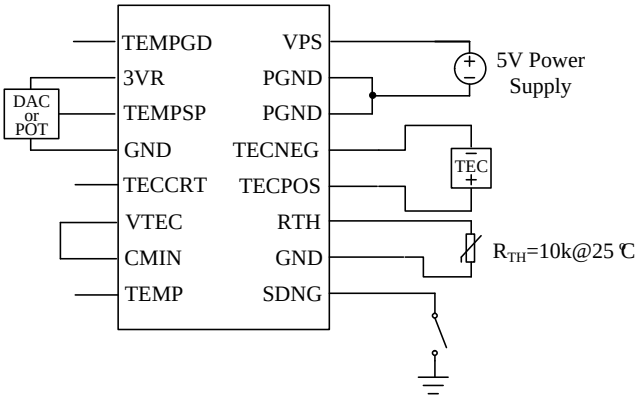


Figure 8. Control the Current Direction of the TEC Module by Pin 3 TEMPSP

When $V_{TECPOS}-V_{TECNEG} > 0$, it is forward current, which cools the object down;
When $V_{TECPOS}-V_{TECNEG} < 0$, it is reverse current, which heats the object up;

The relationship between $V_{TEMPSP}$ and ($V_{TECPOS}-V_{TECNEG}$) is: ($V_{TECPOS}-V_{TECNEG}$) = ($-V_{HTMAX}/V_{VPS}$) ×2 ×$V_{TEMPSP}$+$V_{HTMAX}$
For example, TECA1-5V-3V-DAH, when $V_{TEMPSP}$=2V, ($V_{TECPOS}-V_{TECNEG}$) = (–3/5) ×2 ×2+3 = 0.6V. Note: $V_{TEMPSP}$=0V~$V_{VPS}$

## TYPICAL CHARACTERISTICS

Table 4. Measurement Data of Rth vs. Temperature

| Temperature (℃) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Rth (kΩ) | 32.74 | 31.1 | 29.57 | 28.11 | 26.73 | 25.43 | 24.21 | 23.04 | 21.94 | 20.91 | 19.92 | 18.98 | 18.1 | 17.26 | 16.47 | 15.72 | 15 |
| Temperature (℃) | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 |
| Rth (kΩ) | 14.33 | 13.68 | 13.07 | 12.49 | 11.94 | 11.42 | 10.92 | 10.45 | 10 | 9.57 | 9.17 | 8.78 | 8.41 | 8.06 | 7.72 | 7.40 | 7.10 |
| Temperature (℃) | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 |
| Rth (kΩ) | 6.81 | 6.53 | 6.27 | 6.02 | 5.78 | 5.55 | 5.33 | 5.12 | 4.92 | 4.73 | 4.55 | 4.37 | 4.21 | 4.05 | 3.89 | 3.75 | 3.61 |

Table 5. Measurement Data of Rth vs. $V_{TEMP.}$

| $V_{TEMP}$ (V) | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 | 1.0 | 1.1 | 1.2 | 1.3 | 1.4 | 1.5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Rth (kΩ) | 15.72 | 14.80 | 14.33 | 13.91 | 13.49 | 13.07 | 12.70 | 12.32 | 11.94 | 11.60 | 11.26 | 10.92 | 10.62 | 10.31 | 10.00 |
| $V_{TEMP}$ (V) | 1.6 | 1.7 | 1.8 | 1.9 | 2.0 | 2.1 | 2.2 | 2.3 | 2.4 | 2.5 | 2.6 | 2.7 | 2.8 | 2.9 | 3.0 |
| Rth (kΩ) | 9.73 | 9.45 | 9.17 | 8.91 | 8.66 | 8.41 | 8.18 | 7.95 | 7.72 | 7.52 | 7.31 | 7.10 | 6.91 | 6.72 | 6.53 |

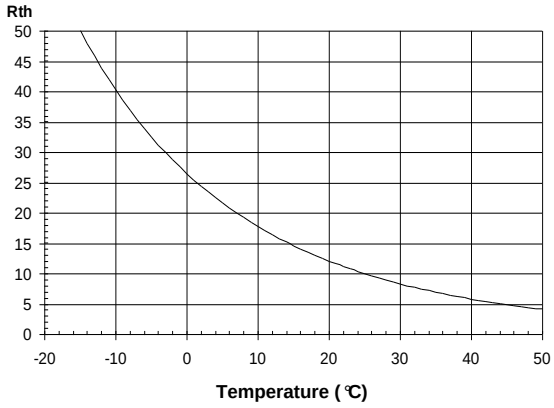


Figure 9. Rth vs. Temperature

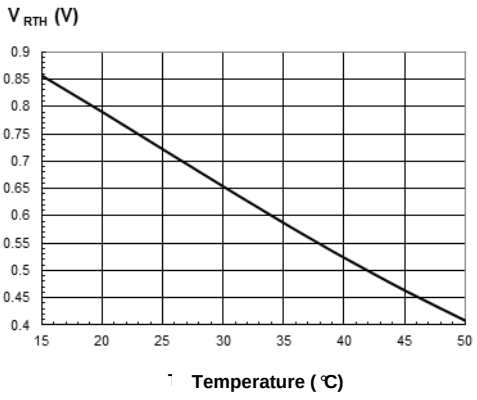


Figure 10. $V_{RTH}$ vs. Temperature

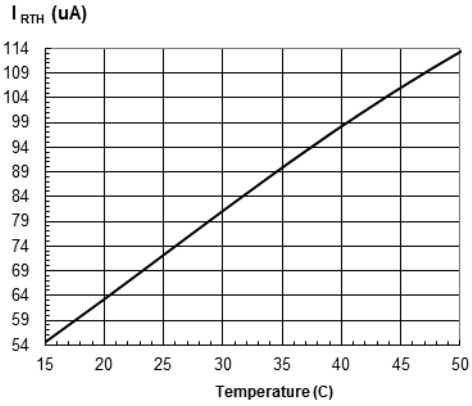


Figure 11. $I_{RTH}$ vs. Temperature

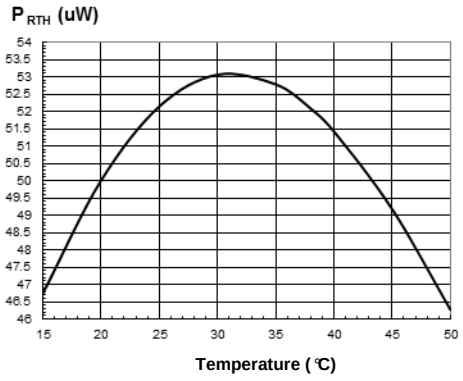


Figure 12. $P_{RTH}$ vs. Temperature

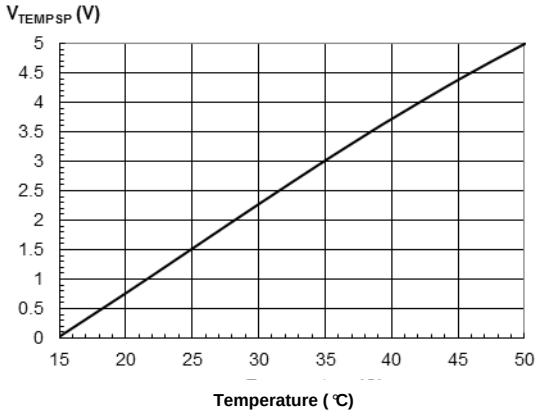


Figure 13. $V_{TEMPSP}$ vs. Temperature

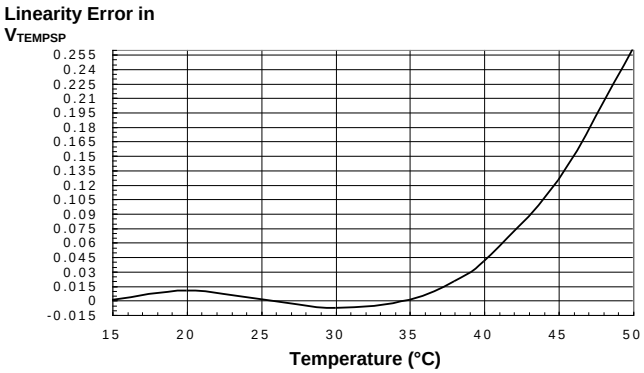


Figure 14.Linearity Error in $V_{TEMPSP}$ vs. Temperature

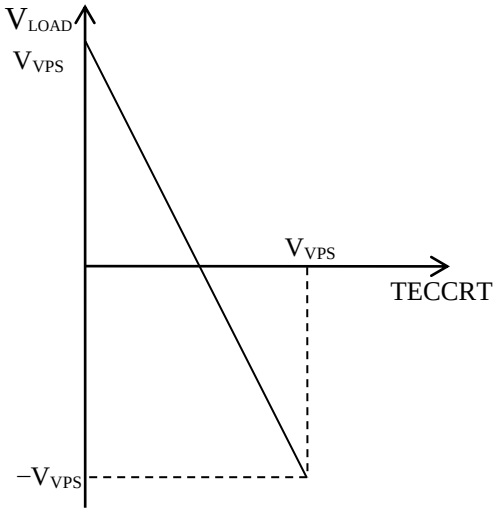


Figure 15. $V_{LOAD}$ vs. TECCRT

Figure 15 shows the relationship between $V_{LOAD}$ and TECCRT. With the increase of the voltage of TECCRT pin, $V_{LOAD}$ will decrease linearly. The approximate formula is $V_{LOAD}$ = TECPOS – TECNEG. When the TECCRT voltage reaches half of $V_{VPS}$, $V_{LOAD}$ is zero; when reaches $V_{VPS}$, the voltage will be $–V_{VPS}$.

Figure 16 shows how VPS and temperature affect the quiescent current ($I_Q$)

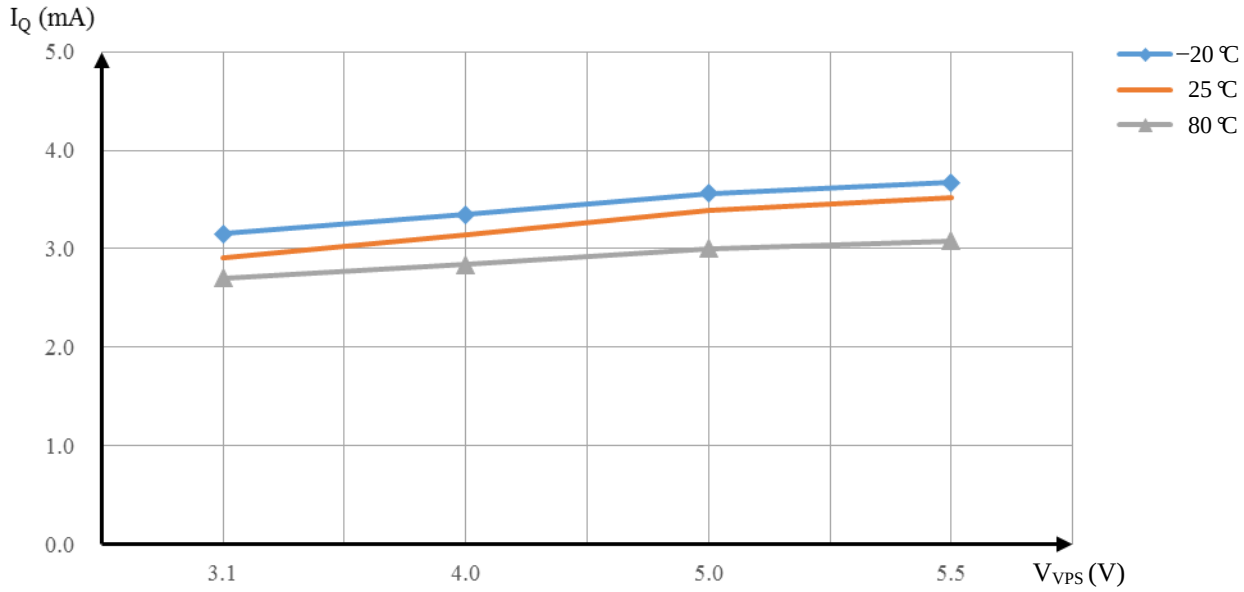


Figure 16. VPS and Temperature vs. $I_Q$

In order to conveniently show the customers the characteristics of TECA1-xV-xV-DAH, we offer the efficiency curves. Figure 17 show the relation between Output Voltage and Efficiency. Figure 18 shows the relation between Output Current and Efficiency.

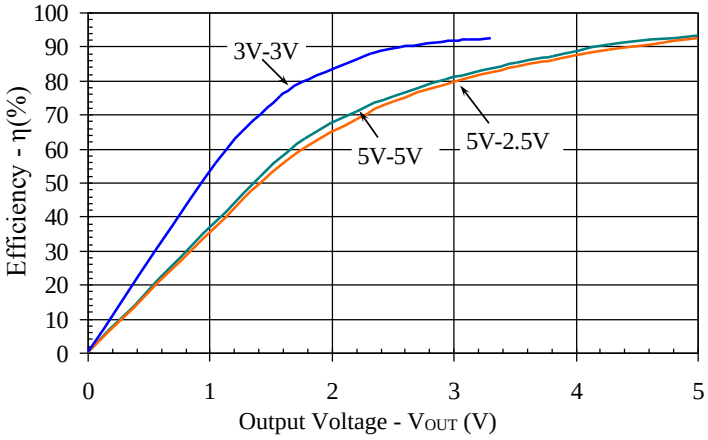


Figure 17. Efficiency vs. $V_{OUT}$

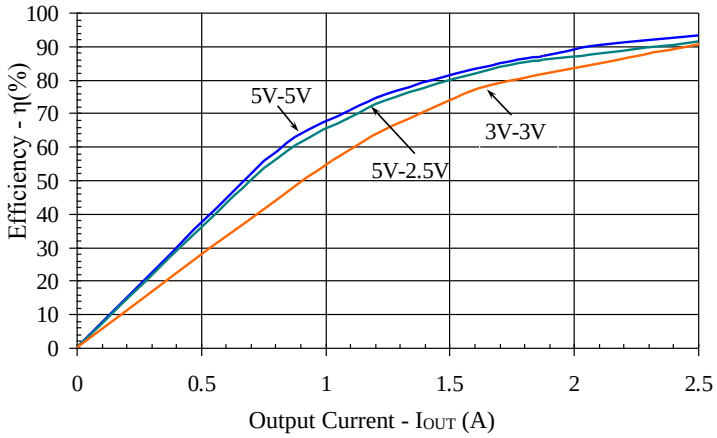


Figure 18. Efficiency vs. $I_{OUT}$

**TEMPGD INTERNAL CIRCUIT**

When temperature difference between the actual temperature and the set-point temperature < 0.1℃, the pull-up resistor R1 for TEMPGD pin is 130Ω; When temperature difference between the actual temperature and the set-point temperature > 0.1℃, the pull-down resistor R2 for TEMPGD pin is 90Ω. See Figure 19.

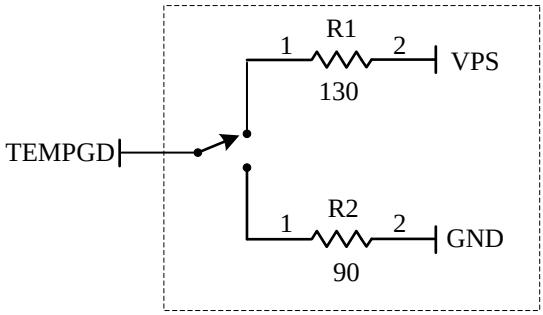


Figure 19. Internal Equivalent Circuit on TEMPGD Pin

## OVERRIDE INTERNAL VOLTAGE SETTING

When the controller does not connect anything externally, the $V_{TEMPSP}$ is 1.5V. If the controller connects a DAC or Potentiometer externally, remove the two 100kΩ resistors in the circuit in Figure 20. Please note that these two resistors are 10MΩ before June 26, 2022, and will be changed to 100kΩ after this date.

For applications that do not need the internal resistors in Figure 20, the part number becomes TECA1-xV-xV-DAH-OP.

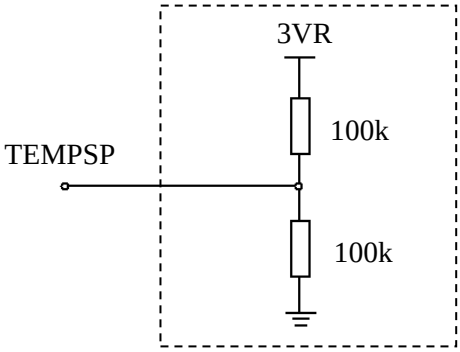


Figure 20. Internal Equivalent Circuit on TEMPSP Pin

## QUIESCENT CURRENT VS. SHUTDOWN VOLTAGE

Figure 21 shows how the quiescent current ($I_Q$) changes with the voltage of Pin SDNG ($V_{SDNG}$).

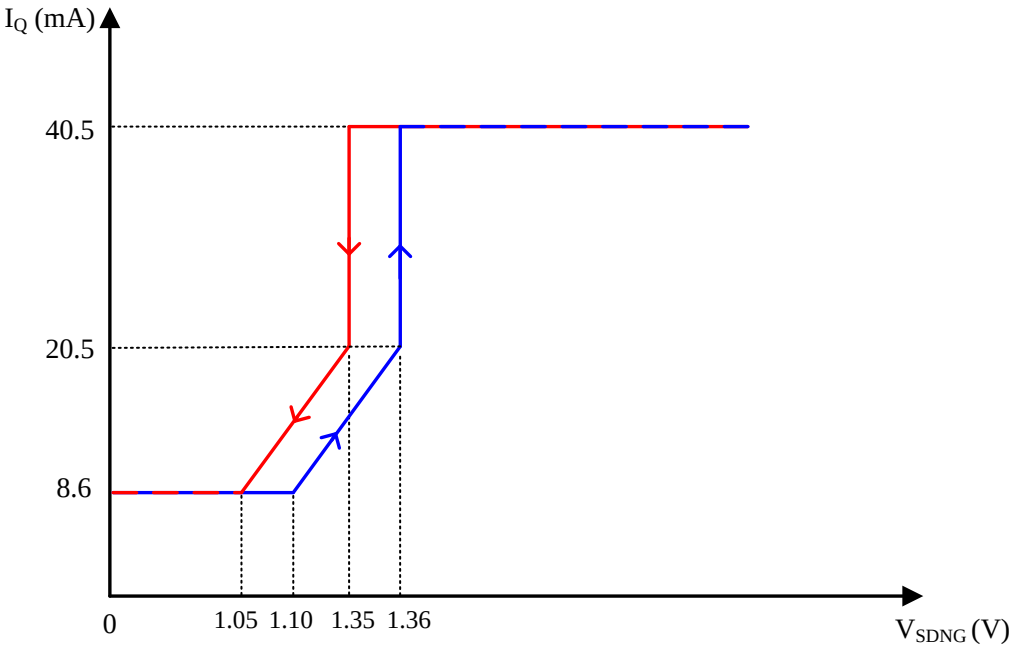


Figure 21. $I_Q$ vs. $V_{SDNG}$

## MECHANICAL DIMENSIONS

The controller comes in only one package: through hole mount. It is often called DIP (Dual Inline package) or D (short for DIP) package and has a part number: TECA1-xV-xV-DAH. Dimensions of the DIP package controller are shown in Figure 22.

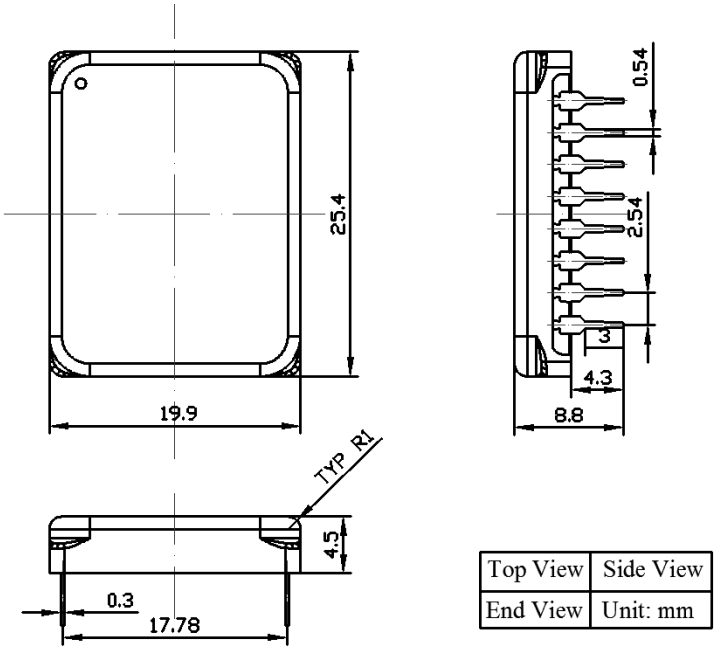


Figure 22. Dimensions of the DIP package controller of TECA1-xV-xV-DAH

## CUSTOMIZATIONS

It is often found that some of the default specifications do not meet our users' particular need. We offer customizations on these specifications:

1. Maximum output voltage across TEC. When ordering, the part number will become: TECA1-5V-(max. TEC voltage)-DAH. E.g., TECA1-5V-2.5V-DAH
2. Set-point temperature range. When ordering, specify the lower limit, the upper limit, and the open circuit temperature. The part number will become: TECA1-5V-2.5V- (lower temp. limit)/(upper temp. limit)/(open circuit temp.), where lower temp. limit is the temperature corresponding to **TEMPSP** = 0V; upper temp. limit is the corresponding to **TEMPSP** = 3V; open circuit temp. corresponding to **TEMPSP** = 1.5V or being left unconnected. e.g., TECA1-5V-2.5V-DAH (20/80/50).
3. Asymmetrical maximum TEC voltage. The maximum TEC voltage for heating and cooling are not the same. When ordering, the part number will become: TECA1-5V- (max. TEC voltage for cooling/Max. TEC voltage for heating), e.g. TECA1-5V-2.5V/1.5V-DAH.

**WARNING: This controller module can only be soldered manually on the board by a solder iron at < 310°C (590°F), it cannot go through a reflow oven process.**

**NOTE: The power supply may have overshoot, when happens, it may exceed the maximum allowed input voltage, 6V, of the controller and damage the controller permanently. To avoid this from happening, do the following:**

1. **Connect the controller solid well with the power supply before turning on the power.**
2. **Make sure that the power supply has sufficient output current. It is suggested that the power supply can supply 1.2 to 1.5 times the maximum current the controller requires.**
3. **When using a bench top power supply, set the current limit to >1.5 times higher than the maximum current the controller requires.**

## SELECTION GUIDE

| Part # | $V_{IN}$ | $V_{OUT}$ | Dimensions (mm) | Difference |
|---|---|---|---|---|
| TEC14M5V3R5AS | 2.7V ~ 5.5V | $\pm V_{VPS}$ | 14.0×14.0×2.2 | Micro TEC controller |
| TEC18V15A | 6.0V~18V | ±15V | 35.7×35.7×7.2 | High voltage high current with embedded firmware inside |
| TEC50V20ACH Under Development | 12V ~ 50V | ±40V | 63.0×61.0×16.7 | High voltage high current |
| TEC5V6A-D | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Linear; TECPOS: Filtered PWM;<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 5mV$ |
| TEC5V6A-DA | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Linear; TECPOS: Filtered PWM<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 2mV$ |
| TEC5V6A-DAH | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Linear; TECPOS: Filtered PWM<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 0.5mV$ |
| TEC5V6A-NT | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Linear; TECPOS: Filtered PWM<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>No internal temperature range setting network |
| TEC5V4A-D | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Linear; TECPOS: Filtered PWM<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 5mV$ |
| TEC5V4A-DA | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Linear; TECPOS: Filtered PWM<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 2mV$ |
| TEC5V4A-DAH | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Linear; TECPOS: Filtered PWM<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$ |
| TEC5V4A-NT | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Linear; TECPOS: Filtered PWM<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>No internal temperature range setting network |
| TECA1-xV-xV-DAH | 3.3V/5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains on @SDNG=0<br>TECNEG: Filtered PWM; TECPOS: Linear<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$ |
| TECA1-xV-xV-DAH-OP | 3.3V/5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains off @SDNG=0<br>TECNEG: Filtered PWM; TECPOS: Linear<br>Two 100kΩ resistors on TEMPSP pin: removed<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$ |

| | | | | |
|---|---|---|---|---|
| TECA1LD-xV-xV-DAH | 3.3V/5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains off @SDNG=0<br>TECNEG: Filtered PWM; TECPOS: Linear<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>With internal compensation network<br>Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \le 0.5mV$ |
| TECA1-xV-xV-D | 3.3V/5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains off @SDNG=0<br>TECNEG: Filtered PWM; TECPOS: Linear<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Max. $\lvert V_{TEMP - VTEMPSP}\rvert \le 5mV$ |
| TECA1-xV-xV-D-OP | 3.3V/5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains off @SDNG=0<br>TECNEG: Filtered PWM; TECPOS: Linear<br>Two 100kΩ resistors on TEMPSP pin: removed<br>Max. $\lvert V_{TEMP - VTEMPSP}\rvert \le 5mV$ |
| TECA1LD-xV-xV-D | 3.3V/5.5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains off @SDNG=0<br>TECNEG: Filtered PWM; TECPOS: Linear<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>With internal compensation network<br>Max. $\lvert V_{TEMP - VTEMPSP}\rvert \le 5mV$ |
| TECA1-5V5V-NT | 5V | $\pm V_{VPS}$ | 25.4×19.9×8.8 | TEMP pin remains off @SDNG=0<br>TECNEG: Filtered PWM; TECPOS: Linear<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>No internal temperature range setting network |
| TECA2-xV-xV-DAH | 4.5V ~ 5.5V | $\pm V_{VPS}$ | 20.14×14.6×8.0 | TEMP pin remains off @SDNG=0<br>TECNEG: Filtered PWM; TECPOS: Linear<br>Two 100kΩ resistors on TEMPSP pin: Not removed<br>Smaller size |

## ORDERING INFORMATION

Table 6. Part number

| Part Number | Description |
|---|---|
| TECA1-xV-xV-DAH | TEMP pin remains on @SDNG=0 |

Table 7. Ordering info.

| Part Number | Description | Difference | Note |
|---|---|---|---|
| TECA1-5V-xV*-DAH | 5V power supply in DIP package with internal net. | No internal compensation network | Voltage difference between TEMP and TEMPSP is −0.02mV ~ 0.5mV, ten times lower than TECA1-5V-xV-D, 4~5mV. |
| TECA1LD-5V-xV*-DAH | | With internal compensation network | |
| TECA1-3V-xV*-DAH | 3.3V power supply in DIP package with internal net. | No internal compensation network | Voltage difference between TEMP and TEMPSP is −0.02mV ~ 0.5mV, ten times lower than TECA1-3V-xV-D, 4~5mV. |
| TECA1LD-3V-xV*-DAH | | With internal compensation network | |
| TECA1-xV-xV*-DAH-OP | | Remove two 100kΩ internal resistors; DIP package | Maximum output voltage across TEC can be selected from 5V, 4.8V, 4V, 3.5V, 3V, 2.5V and 2V or required one. |

*xV stands for the maximum output voltage across TEC. e.g., TECA1-5V-3.5V-DAH

## SPECIAL NOTE

If you experience a high current spike when you change TEMPSP voltage quickly by a large amount, such as > 0.1V, a capacitor of 1 µF can be added between TECCRT and GND. For TEC controllers manufactured after Nov. 10, 2015, there is no such a problem.

**NOTICE**

1. ATI warrants performance of its products for one year to the specifications applicable at the time of sale, except for those being damaged by excessive abuse. Products found not meeting the specifications within one year from the date of sale can be exchanged free of charge.
2. ATI reserves the right to make changes to its products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete.
3. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability. Testing and other quality control techniques are utilized to the extent ATI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.
4. Customers are responsible for their applications using ATI components. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customers to minimize inherent or procedural hazards. ATI assumes no liability for applications assistance or customer product design.
5. ATI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of ATI covering or relating to any combination, machine, or process in which such products or services might be or are used. ATI's publication of information regarding any third party's products or services does not constitute ATI's approval, warranty or endorsement thereof.
6. IP (Intellectual Property) Ownership: ATI retains the ownership of full rights for special technologies and/or techniques embedded in its products, the designs for mechanics, optics, plus all modifications, improvements, and inventions made by ATI for its products and/or projects.